UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,492	11/14/2003	Douglas J. McKenney	03-0085	9210

24319 7590 09/05/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,492	MCKENNEY ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claims 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

2. As for claim 1, applicant claims a method to design an integrated semiconductor product without producing a useful, concrete, and tangible result, see M.P.E.P 2106 [R-3], section II, subsection A. As for claim 1, applicant claims determining steps that do not actually result in a concrete, tangible, and useful result. The determining steps do not actually achieve a final result of design, the final determination step does not actually produce a result. Further, applicant supports the possibility of not actually completing steps in the specification; for example, in paragraphs 0018-0019, where applicant discloses that steps "may" be done. There is no inherent completion of the selecting of transistor threshold voltages as claimed.

Further, claims 10 and 18 appears to be directed to just a data structure as defined IEEE in section IV of M.P.E.P 2106 [R-3].

3. For applicants convenience, copies of pertinent sections are provided below.

M.P.E.P 2106 [R-3], section II, subsection A

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to

inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

Apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement. See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036. Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

M.P.E.P 2106 [R-3] section IV.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material."

Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data

structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, and 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Reuland (US Patent Application Publication 2004/0111690).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

5. As for the claims, Reuland discloses the invention as claimed, including:

A method to design an integrated semiconductor product, comprising:
(a) inputting a description of a range of processing functions into a slice description, the slice description comprising a transistor fabric, and/or at least one hardmac memory [abstract; figs. 1, 4, paragraphs 0002, 0004, 0006];
(b) determining if the range of processing functions has a plurality of memory requirements [fig. 1, paragraph 0007]; and
determining a largest common memory that can satisfy the range of processing functions and the plurality of memory requirements [paragraphs 0021-0024, 0032, 0038];
embedding the largest common memory into the at least one hardmac memory [paragraph 0035, 0002];
embedding at least one embodiment of the range of processing functions into the slice description [paragraph 0038, 0002];
generating register transfer logic from the transistor fabric so that one of the range of processing functions can use a first portion of the largest common memory [paragraphs 0031, 0019, 0035];
wherein the register transfer logic further comprises logic for a port to access the first portion of memory used by the one of the range of processing functions [paragraphs 0031, 0019, 0035, 0021-0024];
wherein a first portion of the largest common memory to be used by one of the range of processing functions is a tightly coupled memory [paragraphs 0021-0024];
(a) identifying a second portion of the largest common memory not used by one of the range of processing functions [paragraphs 0015-0017];
(b) generating register transfer logic to create an additional function from the transistor fabric [paragraphs 0015-0017; 0031, 0019, 0033-0035];
(c) generating register transfer logic to create an additional register and/or memory from the second portion of the largest common memory [paragraphs 0015-0017; 0031, 0019];

(c) generating the interconnect register transfer logic to connect the additional register and or memory to the additional function [paragraphs 0015-0017; 0031, 0019, 0033-0035];
(d) adding the interconnect and the generated register transfer logic to the slice description [paragraphs 0015-0017; 0031, 0019, 0033-0035, 0038];
An article of manufacture, comprising a data storage medium tangibly embodying a program of machine readable instructions executable by an electronic processing apparatus to perform method steps for operating an electronic processing apparatus, said method steps comprising the steps of:
(a) reading a plurality of input files relating to a plurality of embodiments of processing functions that could be incorporated into a design of a partially manufactured semiconductor product having a transistor fabric [abstract; figs. 1, 4, paragraphs 0002, 0004, 0006];
(b) determining the largest common superset of memory that can be used by all of the plurality of embodiments of the processing function [paragraphs 0021-0024, 0032, 0038];
(c) embedding the superset of memory into the design of the partially manufactured semiconductor product [paragraph 0035, 0002];
(d) generating a plurality of output files to configure the embedded memory superset for use by a selected embodiment of the plurality of processing functions [paragraph 0037]; and
(e) updating the design of the partially manufactured semiconductor product with the output files [paragraph 0037];
wherein the output files comprise register transfer logic to tie off any portion of the embedded memory superset not used by the selected embodiment of the plurality of processing functions [paragraph 0037; 0031];
wherein the output files comprise register transfer logic to convert a portion of the transistor fabric to access the embedded memory superset used by the selected embodiment of the plurality of processing functions [paragraph 0037; 0031; 0021-0024];
A method of configuring a partially manufactured semiconductor product having a

transistor fabric and embedded with a memory superset capable of satisfying the memory/register requirements of all of a range .of processing functions, the method of configuring comprising the steps of :

(a) selecting one processing function from the range of processing functions [abstract; figs. 1, 4, paragraphs 0002, 0004, 0006; 0016];

(b) determining how the memory superset is to be apportioned to the selected one processing function [abstract; figs. 1, 4, paragraphs 0002, 0004, 0006; 0016, 0021-0024];

(c) apportioning the memory superset [abstract; figs. 1, 4, paragraphs 0002, 0004, 0006; 0016, 0021-0024];

(d) tying off that portion of the memory superset that is not apportioned [paragraphs 0021; 0031];

(e) determining how to access the apportioned memory superset [paragraphs 0021-0024, 0033];

(f) creating logic within the transistor fabric to access the apportioned memory superset [paragraphs 0021-0024, 0033];

A system to design a partially manufactured semiconductor product, comprising:

(a) means to receive a functional description of the partially manufactured semiconductor product [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];

(b) means to determine if the functional description may include a range of processing functions [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];

means to evaluate the memory and/or register requirements of the range of processing functions [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];

(d) means to specify a memory superset configurable for a memory and/or register requirement for all of the processing functions in the range [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above]; and

(f) means to embed the memory superset into the partially manufactured semiconductor product [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];
(a) means to configure the memory superset into the memory and/or register requirement for one or more of the processing functions in the range [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];
(b) means to create the logic necessary to access the memory and/or register requirement for one or more of the processing functions in the range [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];
A partially manufactured semiconductor product, comprising:
(a) a plurality of functional areas, at least one of the functional areas embedded into the semiconductor product as a configurable superset of semiconductor memory [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];
(b) at least another of the functional areas reserved for one of a range of processing circuits, each one of the range of processing circuits capable of using all or a portion of the configurable superset of semiconductor memory [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above];
(c) configuration logic capable of fulfilling a memory/register requirement of at least one of the range of processing circuits from the configurable superset of semiconductor memory [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above]; and
(d) port logic capable of accessing the memory/register requirement fulfilled from the configurable superset of semiconductor memory [see as rejected for the correspondingly similar limitations of claims 1-5, and 12-17 above].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being obvious over Reuland (US Patent Application Publication 2004/0111690) in view of Janik (US Patent Application Publication 2001/0010073).

The applied reference '690 has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

7. As for the claims, Reuland discloses the invention substantially as claimed, including the method of designing an integrated semiconductor product as cited above in the rejection of claims 1-5, including the largest common memory and range of processing functions.

Reuland does not specifically disclose
wherein the first portion of the largest common memory to be used by one of the range of processing functions is an instruction cache [];
wherein a second portion of the largest common memory to be used by one of the range of processing functions contains tags/addresses for instructions in the instruction cache [];
wherein a second portion of the largest common memory to be used by one of the range of processing functions is a valid register indicating valid and/or invalid instructions in the instruction cache [];
wherein the first portion of the largest common memory to be used by one of the range of processing functions is a data cache [];
wherein a second portion of the largest common memory to be used by one of the range of processing functions contains tags/addresses for data in the data cache [];
wherein a second portion of the largest common memory to be used by one of the range of processing functions is a valid register indicating which data in the data cache is or is not valid [];

Janik discloses the use of instruction/ data cache as well as valid register [paragraphs 0059 and 0085].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Reuland and Janik because utilizing the use of instruction/ data caches as well as valid registers within Reuland's system would have provided Reuland's system with memory and register configurations that are useful in the design and implementation of pipelined, speculative processor applications, which would provide for faster, and more reliable instruction/ data execution within a designed circuit [see Janik, abstract; paragraphs 0059, and 0085].

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
August 30, 2006